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AVT-718 - Hardware Revisions "D" and "D2"

This hardware revision separates the power source for K-line communications (both KWP and UBP modes) from the power source for the unit and all other modes of communications.

Important Note

Hardware revision "D" of the AVT-718 was created to fill a unique need. Regular production units are not modified to this hardware revision level unless explicitly requested by a customer.

Introduction

In an 'ordinary' AVT-718 unit the input power, "V-BATT", enters the AVT-718 unit on the D-15P connector P3 pin #13. This input power source is the reference for the K-line transmitters and receivers for KWP mode and UBP mode.

Remember that all K-line communications use the V-BATT voltage as a reference, it is not regulated or controlled.

The same V-BATT input power source also directly supplies the J1850 VPW transceiver and the Single Wire CAN (SWC) transceiver. However, these transceivers incorporate internal voltage regulators to control the waveform voltage.

The V-BATT input power source also supplies a wide input range DC/DC converter to provide the +5v power to all board logic circuits.

Hardware Revision "D"

Hardware revision "D" separates the K-line power source from the rest of the board power requirements. Two changes are made to the board to accomplish this; they are described below.

The resulting configuration for the AVT-718 is listed on the next page.

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Revision "D2" Configuration

Hardware revision "D2" was created to convert a revision "C" or "F" board to be compatible with the AVT-718 revision "G" board (with jumper selected K-line power).

- P3 pin #13 is "Unit Power" [same as a 'regular' board].
  This input power source supplies all modes of operation that do not use the K-line (VPW, PWM, and CAN) and supplies all board logic circuits.
- "Unit Power" input voltage range is: +9v to +36v.
- "Unit Power" input is switched, fused, and input over-voltage protected.

- P3 pin #1 is "K-line Power".
  This power source supplies the K-line receiver and transmitter for KWP mode of operation. It also supplies the UPL transceiver for UBP and LIN modes of operation.
- "V-BATT" input voltage range is approximately +8v to +24v.
- Note that "V-BATT" is not: switched, fused, or input over-voltage protected.

Connector P3 and Jumper JP1 Summary

P3 Pin #	Where to	Description	OBD-II Connector [using AVT OBD-II cable]
1	JP1 pin 19	"K-line" power input Rev. "D2" only	
2	JP1 pin 2 JP1 pin 4		J1850 bus +
3	JP1 pin 18		
4	*ground plane*	Ground	Ground
5	*ground plane*	Ground	Ground
6	JP1 pin 12		
7	JP1 pin 8		K-line
8	JP1 pin 20		
9	JP1 pin 16		
10	JP1 pin 6		J1850 bus -
11	JP1 pin 21		
12	JP1 pin 22		
13	*power input protection circuit*	"Unit Power"	+V-BATT
14	JP1 pin 14		
15	JP1 pin 10		L-line

Hardware Modifications

The following describes the hardware modification required to convert a revision “D” unit to revision “D2” configuration.

- Remove all ‘white’ wires from the bottom of the board.
- On the top layer (L1) connect a wire from D25 cathode to U31-8.
  [Reconnect the cut trace.]
- On the top layer (L1) cut the trace from D26 cathode to C55.
- Using a 1N5819 diode covered in heat shrink:
  connect the anode to P3 pin #1
  connect the cathode to R119.
- Using a white wire connect R120 to a via of the short ‘fat’ trace directly under U7.

The following describes the hardware modification required to convert a revision “C” or “F” unit to revision “D2” configuration.

- On internal layer 5 (L5) cut the trace leading from U30 (DC/DC converter) pin #1 to R120 (through-hole resistor).
  [Cutting the internal layer trace is a tricky operation.]
- On the top layer (L1) cut the trace from D26 cathode to C55.
- Using a 1N5819 diode covered in heat shrink:
  connect the anode to P3 pin #1
  connect the cathode to R119.
- Using a white wire connect R120 to a via of the short ‘fat’ trace directly under U7.

Questions ??

Contact AVT directly if there are any questions.

Our contact information is provided at the bottom of page 1 and is available from our web site
http://www.avt-hq.com

Revision "D" Configuration

- P3 pin #13 is "V-BATT".
  This power source supplies the K-line receiver and transmitter for KWP mode of operation. It also supplies the UPL transceiver for UBP mode of operation.
- "V-BATT" input voltage range is approximately +5v to +34v.
- Note that "V-BATT" is: switched, fused, and input over-voltage protected.

- P3 pin #1 is "Unit Power".
  This input power source supplies all other modes of operation and supplies all board logic circuits.
- "Unit Power" input voltage range is: +9v to +36v.
- Note that "Unit Power" is: not switched, not fused, and not input over-voltage protected.

Connector P3 and Jumper JP1 Summary

P3 Pin #	Where to	Description	OBD-II Connector [using AVT OBD-II cable]
1	JP1 pin 19	"Unit Power" input Rev. "D" only	
2	JP1 pin 2 JP1 pin 4		J1850 bus +
3	JP1 pin 18		
4	*ground plane*	Ground	Ground
5	*ground plane*	Ground	Ground
6	JP1 pin 12		
7	JP1 pin 8		K-line
8	JP1 pin 20		
9	JP1 pin 16		
10	JP1 pin 6		J1850 bus -
11	JP1 pin 21		
12	JP1 pin 22		
13	*power input protection circuit*	+V-BATT	+V-BATT
14	JP1 pin 14		
15	JP1 pin 10		L-line

Hardware Modifications

The following describes the actual hardware modification to implement hardware revision “D”.

- On the top layer (L1) cut the trace from D25 cathode leading to U31-8.
- On internal layer 5 (L5) cut the trace leading from U30 (DC/DC converter) pin #1 to R120 (through-hole resistor).
  [Cutting the internal layer trace is a tricky operation.]
- On the bottom of the board connect a wire from pin #1 of U30, the DC/DC converter, to P3 pin #1.
- On the bottom of the board connect a wire from R120 (the cut trace on L5) to the cathode of D25.

Questions ??

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