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HBCC (PWM) Interrupt Register Definitions

Most AVT interface units, when in PWM mode, use the HBCC (Hosted Bus Controller Chip) to implement Ford Motor Company SCP (Standard Corporate Protocol).

There are three error/status messages that the AVT interface may generate and send to the host during operations. With each of these three error/status messages the contents of the associated interrupt register is sent.

A description of each error/status message and the corresponding interrupt register contents is provided in this document.

Note that all numbers used here are HEX.

All of the following register and bit descriptions provided below are exact quotations from the HBCC User's Manual and are provided courtesy of the Ford Motor Company.

Comments inserted by AVT are presented in [brackets].

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Error/Status message

22 08 xx where xx = IR1 value

Interrupt Register 1 (IR1) bit definitions

Bits 2 - 1 - 0: Received byte count, minus 4. The HBCC receiver sets these three bits to indicate the byte count of the received message. The message byte count is actually 4 greater than the binary number indicated, allowing a total message count of 11 bytes. [All SCP messages have at least 4 bytes: Priority/Type, Target specifier, Source address, CRC.]

Bit 3: Not used, always returns zero.

Bit 4: Unable to Acknowledge. This bit indicates that a valid Function, Broadcast, or Node-to-Node message has been received and is in the receiver buffer, but the receiver was unable to acknowledge for any of the following reasons:

- The 101-bit message limit had already been reached.
- The acknowledgment was "arbitrated out" due to lower address acknowledgers consuming all acknowledgment slots.
- A premature end of acknowledgment has been detected (EOD or invalid bit within the acknowledgment byte).

Bit 5: Receiver Overrun. This bit is set by the HBCC to indicate that the Receive Buffer and the HBCC's internal 13-byte receive FIFO memory are both full, and another qualified Function, Broadcast, or Node-to-Node message has appeared on the SCP bus. The new message has been discarded and will not be acknowledged.

Bit 6: Receive Error. This bit indicates that the HBCC receiver has detected an error after the first two bytes of a qualified Function, Broadcast, or Node-to-Node message. The errors detected are Message Too Long (no EOD after 91 bits), CRC error, Invalid PWM bit, and Premature EOD.

Bit 7: Message Received OK. This bit indicates that the Network Receiver has successfully completed the acknowledgment phase of a qualified Broadcast, Function, or Node-to-Node message.

Error/Status message

22 09 xx where xx = IR2 value

Interrupt Register 2 (IR2) bit definitions

Bits 2 - 1 - 0: Acknowledger Count. These three bits indicate the count of acknowledgers collected from the last transmitted message, or the number of returned data bytes including CRC from a Function Read or BCC Access message type. In Monitor Mode, this field indicates the number of acknowledgers in the receive buffer.

Bit 3: Not used, always returns zero.

Bit 4: Network Driver Watchdog Expired. This bit indicates that the Network Driver has held the network in an actively driven state for longer that four bit phase periods, indicating a hardware failure in the Network Driver.

Bit 5: Loss of Arbitration Limit Expired. This bit indicates that the HBCC made seven attempts to transmit a message, but each time detected a loss of arbitration during the first three bytes of the message, indicating loss of arbitration to a higher-priority message.

Bit 6: Transmit Error Limit Expired. This bit indicates that the HBCC made three attempts to transmit a message, but each time encountered a transmit data mismatch, invalid bit or premature EOD error, received no acknowledgment, or (depending on message type) received an invalid acknowledgment.

Bit 7: Message Transmitted OK. This bit indicates a successful transmission of a message and the reception of at least one valid acknowledgment. No bit error, data mismatch error, or returned CRC error (for messages returning data) occurred.

Error/Status message

22 0A xx where xx = IR3 value

Interrupt Register 3 (IR3) bit definitions

Bit 0: Request for Sleep. This bit is set by the HBCC to indicate that 64 seconds have elapsed since the last host-HBCC interaction, network activity, or ... [other activities that are not used in AVT interface products].

Bit 1: Restricted Operation. This bit is set and a non-maskable interrupt is generated if any attempt is made to access a register address greater than 17H. The HBCC contains internal registers beyond 17H which are not used for normal operation.

Bit 2: Network Fault Detected. This bit is set when the HBCC Network Interface has detected a network fault (such as an open or shorted bus conductor). This bit is updated during the SOM phase of each bus message, including those transmitted by this HBCC. The host [microcontroller] may examine the Decode Status bits (bits 4, 5, 6, and 7) of the Host Interface Mode Status Register [register address 13] for diagnostic indication of the nature of the fault.

Bit 3: Wake up from User Input Activity. [User Input pins on the HBCC are not used on AVT interface units. Therefore, this bit will not be set and no interrupt will be generated.]

Bit 4: Wake up from Network Activity. This bit is set by the HBCC to indicate that it has resumed the AWAKE state as a result of detecting activity on the network bus. [AVT interfaces never command the HBCC to SLEEP state.]

Bit 5: Power Interrupted. This bit is set to indicate loss of continuity of HBCC power. The threshold is about 3 volts, such that below that point, data retained in SLEEP mode is questionable.

Bit 6: Not used, always returns zero.

Bit 7: HBCC Reset has Occurred. This bit is set by the HBCC when in completes its RESET sequence, whether caused by host command or by the /RESET pin.

Host Interface Mode Status Register

Register address 13

Bit definitions

Bit 0: MS1. Mode bit.

Bit 1: MS2. Mode bit.

[AVT interface units operate the HBCC in Motorola serial mode.
MS1 = MS2 = '1']

Bit 2: Host Watchdog Expired. This bit is set by the HBCC to indicate that an unmasked interrupt condition has existed for at least 4 seconds without any response from the host [microcontroller]. The HBCC will disable the interrupt signal output pin driver and will ignore all network message types except BCC Access. If the 64-second Sleep Activity Timer has expired, the HBCC will enter SLEEP mode regardless of the state of the Never Sleep and Go To Sleep bits in the HBCC Control Register.

Bit 3: Not used, always returns zero.

Bit 4: SEA status. Singled Ended A line. [Chart below.]

Bit 5: DE status. Differential. [Chart below.]

Bit 6: SEB status. Single Ended B line. [Chart below.]

Bit 7: This Node Transmitting. This bit is set if, during a network fault, this node was driving the network wires. This bit is cleared upon a non-faulted received SOM or a non-faulted transmitted SOM.

SEB	DE	SEA	Description
0	0	0	not used
0	0	1	Bus fault (B stuck passive)
0	1	0	Receiver fault
0	1	1	Bus fault (B stuck active)
1	0	0	Bus fault (A stuck passive)
1	0	1	Receiver fault
1	1	0	Bus fault (A stuck active)
1	1	1	No fault